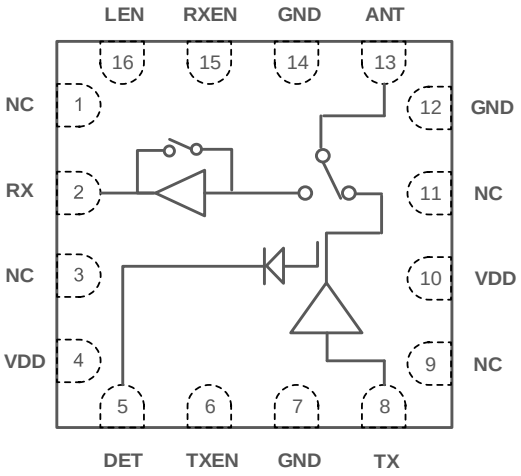
CMOS 5GHz WLAN 802.11ac RFeIC WITH PA, LNA AND SPDT



Description

RFX8051 is a highly integrated, single-chip, single-die RFeIC (RF Front-end Integrated Circuit) which incorporates key RF functionality needed for IEEE 802.11a/n/ac WLAN system operating in the 5.15-5.85GHz range. The RFX8051 architecture integrates a high-efficiency high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network, LO rejection, and harmonic filters all in a CMOS single-chip device.

RFX8051 has simple and low-voltage CMOS control logic, and requires minimal external components. A directional coupler based power detect circuit is also integrated for accurate monitoring of output power from the PA.

RFX8051 is assembled in an ultra-compact low-profile 3.0x3.0x0.55 mm 16-lead QFN package, and is the ideal RF front-end solution for implementing 5GHz WLAN in smartphones and other platforms.

Applications

- 802.11n/ac Wi-Fi Devices
- Tablets / MIDs
- Wi-Fi Media Gateways
- Consumer Electronics
- Notebook / Netbook / Ultrabook
- Access Points / Routers
- Set Top Boxes / Wireless IPTVs
- Other 5GHz ISM Platforms

FEATURES

- 5GHz WLAN Single Chip, Single-Die RF Front-End IC
- High Transmit Signal Linearity Meeting 802.11ac Standard
- Separate TX, RX Transceiver Ports, Single Antenna Port
- 5GHz Power Amplifier with Low-Pass Harmonic Filter
- Low Noise Amplifier with Bypass Mode
- Transmit/Receive Switch Circuitry
- Integrated Power Detector for Transmit Power Monitor and Control
- Low Voltage (1.2V) CMOS Control Logic
- Low DC Power Consumption
- ESD Protection Circuitry on All Pins
- DC Decoupled RF Ports
- Internal RF Decoupling on All VDD Bias Pins
- Low Noise Figure for the Receive Chain
- High Power Capability for Received Signals in Bypass Mode
- Full On-chip Matching Circuitry
- Minimal External Components Required
- 50-Ohm Input / Output Matching
- Market Proven CMOS Technology
- 3mm x 3mm x 0.55mm Small Outline 16L QFN Package with Exposed Ground Pad
- RoHS and REACH Compliant

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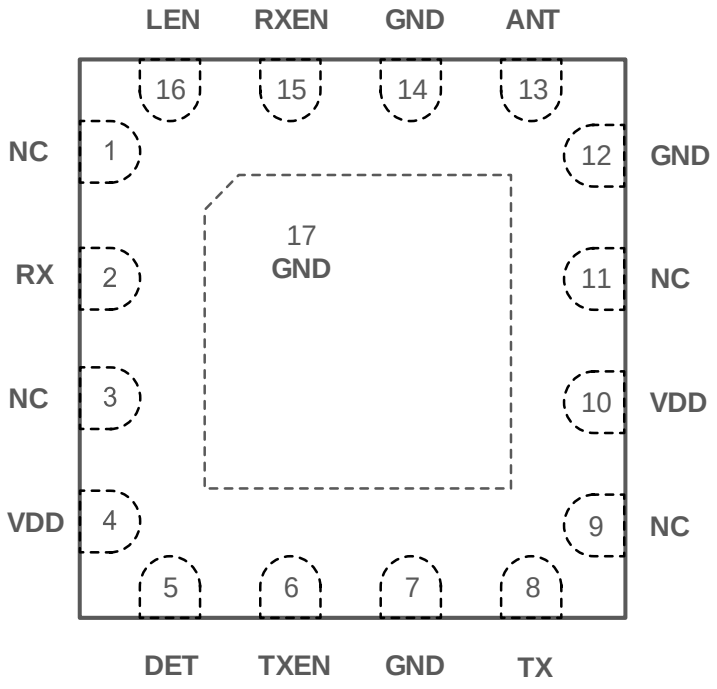
PIN ASSIGNMENTS:

Pin Number	Pin Name	Description
1, 3, 9, 11	NC	Internally Not Connected
2	RX	RF Output Port from LNA or Bypass – DC Shorted to GND
4, 10	VDD	DC Supply Voltage
5	DET	Analog Voltage Proportional to the PA Power Output
6	TXEN	CMOS Input to Control TX Enable
7, 12, 14, 17	GND	Ground – Must Be Connected to GND in the Application Circuit
8	TX	RF Input Port from the Transceiver – DC Shorted to GND
13	ANT	Antenna Port RF Signal from the PA or RF Signal Applied to the LNA – DC Shorted to GND
15	RXEN	CMOS Input to Control RX Enable
16	LEN	CMOS Input to Control LNA Enable or Bypass Mode

PIN-OUT DIAGRAM:



(Top "See-Through" View)

ABSOLUTE MAXIMUM RATINGS:

Parameters	Units	Min	Max	Conditions
DC VDD Voltage Supply	V	0	3.9	All VDD Pins
DC Control Pin Voltage	V	0	3.6	All Control Pins
DC VDD Current Consumption	mA		400	Through VDD Pins when TX is "ON"
TX RF Input Power	dBm		+7	
ANT RF Input Power	dBm		+20	Bypass Mode
Junction Temperature	^oC		150	
Storage Ambient Temperature	^oC	-40	+150	Appropriate care required according to JEDEC Standards
Operating Ambient Temperature	^oC	-40	+85	
Moisture Sensitivity				MSL1
ESD HBM	V	+/-4250		All Pins

Note: Sustained operation at or above the Absolute Maximum Ratings for any one or combinations of the above parameters may result in permanent damage to the device and is not recommended.

All Maximum RF Input Power Ratings assume 50-Ohm terminal impedance.

NOMINAL OPERATING CONDITIONS:

Parameters	Units	Min	Typ	Max	Conditions
DC VDD Voltage Supply *(Note 1)*	V	3.0	3.3	3.6	All VDD Pins
Control Voltage "High" *(Note 2)*	V	1.2		3.3	
Control Voltage "Low"	V	0		0.3	
DC Control Pin Current Consumption	µA		1		
DC Shutdown Current	µA		3		
PA Turn On/Off Time	µsec		0.5	1	
θja *(Note 3)*	^{o}C/W		42		
θjc *(Note 4)*	^{o}C/W		10		
LNA Turn On/Off Time	µsec		0.5	1	
Shut-Down and "ON" State Switching Time	µsec		0.5	1	

Note 1: For normal operation of the RFX8051, VDD must be continuously applied to all VDD supply pins.
Note 2: If control voltage can exceed 1.8V, a 1KΩ – 10KΩ series resistor is recommended for the application circuit on each control line.
Note 3: For operation above +85 ºC, use the Θja as guidance for system design to assure the junction temperature will not exceed the maximum of +150 ºC.
Note 4: Case is defined as the bottom of the EVB under the thermal vias.

TRANSMIT PATH CHARACTERISTICS (VDD=3.3V; T=+25°C)

Parameters	Units	Min	Typ	Max	Conditions
Operating Frequency Band	GHz	5.15		5.85	
Linear Output Power for 802.11ac	dBm		+16		EVM<1.8%, MCS9 256QAM 80MHz
Linear Output Power for 802.11n	dBm		+17		EVM<3%, MCS7 64QAM 40MHz
Linear Output Power for 802.11a	dBm		+17.5		EVM<3%, 64QAM 54Mbps
Linear Output Power for 802.11a 6Mps	dBm		+19		For MCS0/6Mbps Mask Compliace
Small-Signal Power Gain (Pin = -20dBm)	dB	27	28		Between TX and ANT pins
Power Gain Flatness	dB		±0.5		Between TX and ANT pins
Output P_{1dB}	dBm		+23		Between TX and ANT pins
TX Quiescent Current	mA		140		No RF Signal Applied
TX Linear Current	mA		200		P_{OUT} = +17dBm, 20 MHz
Power Detector Voltage Output	V		0.15 - 1		P_{OUT} = +5 to +20dBm, 10kΩ Load
Second Harmonic	dBc		-40		P_{OUT}=+20dBm, CW
Third Harmonic	dBc		-40		P_{OUT}=+20dBm, CW
Input Return Loss	dB		-14		At TX Port
Output Return Loss	dB		-14		At ANT Port
Load VSWR for Stability (CW, Fixed Pin for Pout=+20dBm with 50Ω load)	N/A	4:1	6:1		All non-harmonically related spurs less than -43dBm/MHz
Load VSWR for Ruggedness (CW, Fixed Pin for Pout=+20dBm with 50 Ohm Load)	N/A	8:1	10:1		No Damage

RECEIVE PATH CHARACTERISTICS (VDD=3.3V; T=+25°C)

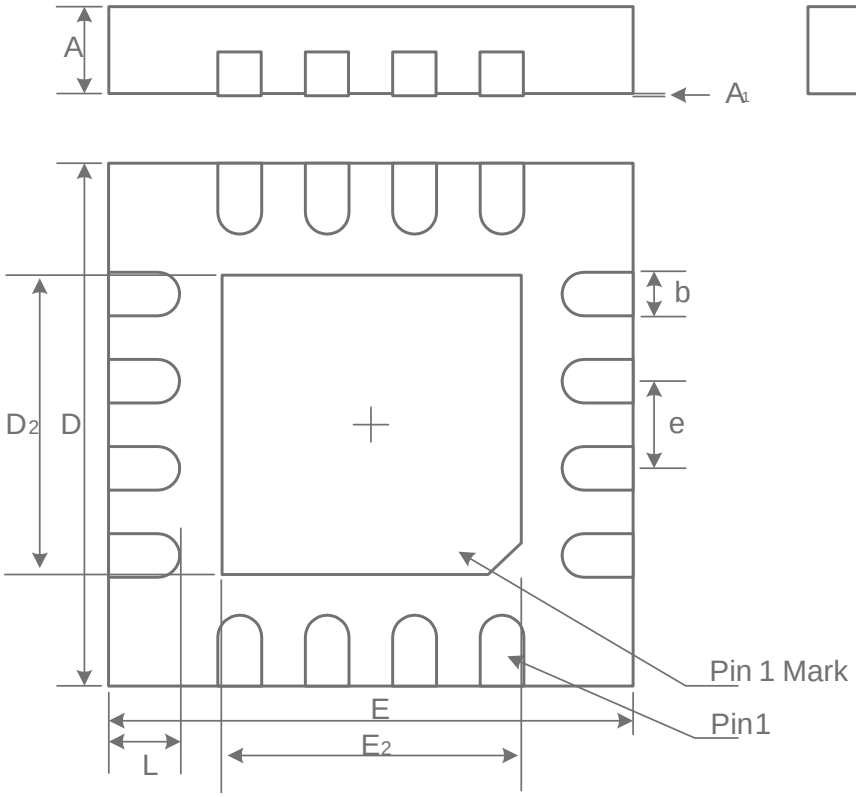
Parameters	Units	Min	Typ	Max	Conditions
Operating Frequency Band	GHz	5.15		5.85	All RF Pins are Loaded by 50-Ohm
Gain	dB		11		Between ANT and RX pins, Low NF Mode; RXEN=LEN="High"
Noise Figure	dB		3		At ANT Pin, Low NF Mode
Insertion Loss for LNA Bypass Mode	dB		6		Between ANT and RX Pins; RXEN="High", LEN="Low"
Input Return Loss	dB		-12		At ANT Port, Low NF Mode
			-12		LNA Bypass Mode
Output Return Loss	dB		-12		At RX Port, Low NF Mode
			-12		LNA Bypass Mode
RF Port Impedance	Ohm		50		
DC Quiescent Current	mA		15		No RF Applied, Through VDD, Low NF Mode
			1.2		No RF Applied, Through VDD, LNA Bypass Mode
Input P_{1dB}	dBm		-5		At ANT Pin, Low NF Mode
			+13		At ANT Pin, LNA Bypass Mode

CONTROL LOGIC TRUTH TABLE

TXEN	LEN	RXEN	Mode Of Operation
0	0	0	Shutdown Mode
1	X	X	Transmit Mode
0	1	1	Low NF Receive Mode
0	0	1	LNA Bypass Receive Mode
All Others			Unsupported (No Damage)

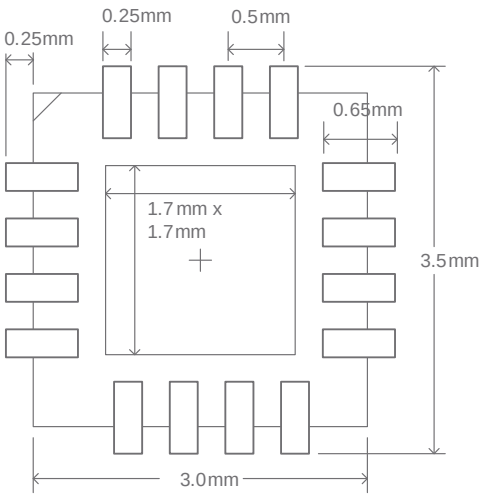
Note: "1" denotes high voltage state (> 1.2V)
"0" denotes low voltage state (<0.3V) at Control Pins
"X" denotes the don't care state
1KΩ – 10KΩ series resistor may be required for each control line

PACKAGE DIMENSIONS (All Dimensions in mm):



Dimensions (mm)			
	Min	Nom	Max
A	0.5	0.55	0.6
A_1	0.00		0.05
b	0.20	0.25	0.30
D	2.95	3.00	3.05
D_2	1.65	1.70	1.75
E	2.95	3.00	3.05
E_2	1.65	1.70	1.75
e	0.45	0.50	0.55
L	0.35	0.40	0.45

PCB LAND PATTERN



PACKAGE MARKING: