PRELIMINARY DATA SHEET

SKY87608: 28 V, 3 A Non-Synchronous Step-Down Converter

Applications

- Set-top boxes
- Distributed power systems
- Industrial applications

Features

- 4.5 V to 28 V input voltage
- Up to 97% efficiency
- Internal 180 mΩ high-side N-channel MOSFET
- Internal 12 Ω refresh MOSFET
- Up to 3 A load current
- Adjustable output voltage (0.9 V to 0.8 × V_{IN})
- Fixed 450 kHz switching frequency
- 4 ms soft-start period
- External compensation
- Less than 1 µA shutdown current
- Current limit protection
- Standard 8-pin SOP-8L package (MSL1, 260 °C per JEDEC-J-STD-020) with exposed pad

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

Description

The SKY87608 is a step-down DC-DC converter that operates with a wide 4.5 V to 28 V input voltage range and regulates the output voltage as low as 0.9 V while supplying up to 3 A to the output. The 450 kHz switching frequency allows for an efficient step-down regulator design.

The SKY87608 uses an adjustable output voltage that can be set from 12% to 80% of the input voltage by an external resistive voltage divider. Internal soft-start prevents excessive inrush current without requiring an external capacitor.

The SKY87608 includes input under-voltage and overcurrent protection to prevent damage in the event of a fault condition. Thermal overload protection prevents damage to the SKY87608 or circuit board when operating beyond its thermal capability.

The SKY87608 is available in a small Pb-free, 8-pin, SOP-8L-EP package.

A typical application circuit is shown in Figure 1. The pin configuration is shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

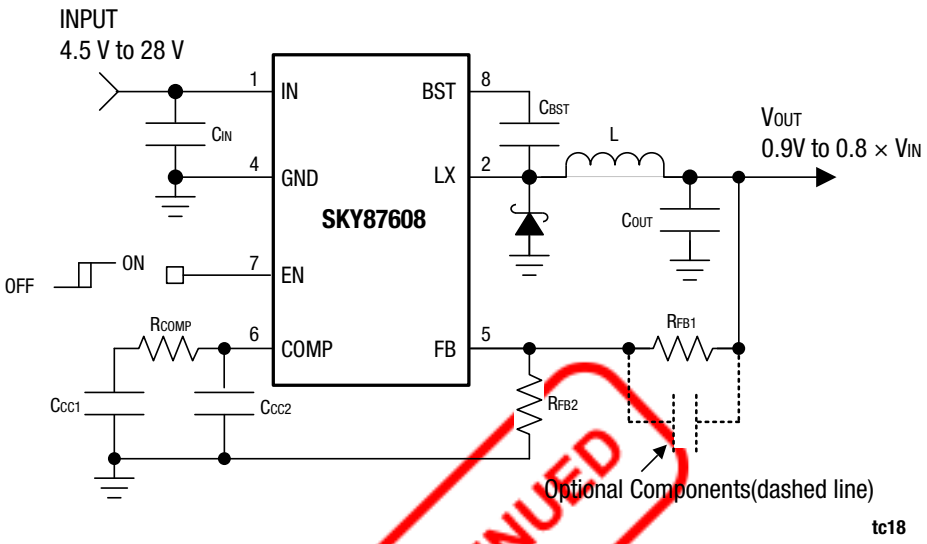


Figure 1. SKY87608 Typical Application Circuit

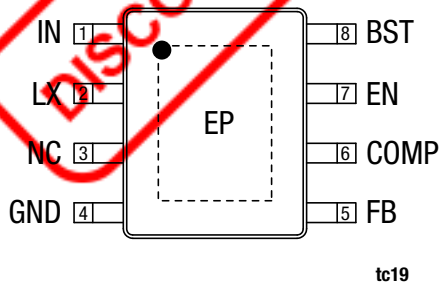


Figure 2. SKY87608 8-Pin SOP-8L
(Top View)

Table 1. SKY87608 Signal Descriptions

Pin #	Name	Description
1	IN	Input supply. Connect IN to the input power source. Bypass IN to GND with a 10 µF or greater ceramic capacitor. IN connects to the source of the internal high-side N-channel MOSFET and linear regulators powering the controller and drivers.
2	LX	Inductor switching. LX is internally connected to the source of the internal high-side N-channel MOS- FET, the high-side driver, and current-sense circuitry. Connect to the power inductor, and the Schottky diode as shown in the Typical Application Circuit diagram.
3	NC	Do NOT connect externally. Leave pin floating.
4	GND	Ground. GND is internally connected to the analog ground of the control circuitry, and the source of the 12 Ω refresh MOSFET.
5	FB	Feedback input. FB senses the output voltage for regulation control. Connect a resistive divider network from the output to FB to GND to set the output voltage accordingly. The FB regulation threshold is 0.9 V for the SKY87608.
6	COMP	Compensation pin of the error amplifier.
7	EN	Enable input. Logic high enables the regulator. A logic low forces the SKY87608 into shutdown mode, placing the output into a high-impedance state and reducing the quiescent current to less than 1 µA.
8	BST	Boot-strapped high-side driver supply. Connect a 0.1 µF ceramic capacitor between BST and LX as shown in the Typical Application Circuit diagram.
–	EP	Exposed paddle. Connect to PCB ground plane.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY87608 are provided in Table 2. Thermal information is provided in Table 3, and electrical specifications are provided in Table 4.

Typical performance characteristics of the SKY87608 are illustrated in Figures 3 through 24.

Table 2. SKY87608 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Maximum	Units
IN to GND voltage	V_{IN}	–0.3	+30	V
LX to GND voltage	V_{LX}	–0.3	V_{IN} + 0.3	V
BST to GND voltage	V_{BST}	V_{CC} – 0.6	V_{IN} + 6	V
EN to GND voltage	V_{EN}	–0.3	+30	V
FB to GND voltage	V_{FB}	–0.3	+6	V
COMP to GND voltage	V_{COMP}	–0.3	+6	V

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 3. SKY87608 Thermal Information (Note 1) (Note 2)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Operating ambient temperature	T_A	–40		+85	°C
Operating junction temperature	T_J	–40		+150	°C
Maximum soldering temperature (at leads, 10 seconds.)	T_{LEAD}		300		°C
SKY87608 SOP-8L-EP Thermal Impedance					
Maximum junction-to-ambient thermal resistance	θ_{JA}		41		°C/W
Maximum power dissipation (Note 3)	P_D		2.8		W

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Note 2: Mounted on 1 inch^2 FR4 board.

Note 3: Derate 27 mW/°C above 25 °C.

Table 4. SKY87608 Electrical Specifications (Note 1)
(V_{IN} = 12 V, V_{EN} = 5 V, AGND = PGND, T_A = –40 °C to 85 °C, Typical Values are at T_A = 25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Input voltage	V_{IN}		4.5		28	V
No load supply current	I_Q	No load current; not switching		1.6	3.2	mA
Shutdown current	I_{SHDN}	EN = GND, V_{IN} = 28 V		1	5	µA
Output voltage (Note 2)	V_{OUT}		0.9		0.8 × V_{IN}	V
Nominal feedback voltage				0.9		V
FB accuracy	V_{FB}	No load, V_{IN} = 24 V	0.88	0.90	0.92	V
FB leakage current	I_{FB}	FB = 1.5 V or GND	–0.2		+0.2	µA
Load regulation	ΔV_{OUT} / I_{OUT}	V_{IN} = 12 V, V_{OUT} = 5 V		1.0		%
Line regulation	ΔV_{OUT} / V_{IN}	V_{IN} = 4.5 V to 28 V		0.5		%
Oscillator frequency	f_{OSC}		380	450	520	kHz
Minimum on-time	$t_{ON(MIN)}$			260		ns
Maximum duty cycle	D_{MAX}	No Load	80	83		%
High-side MOSFET “on” resistance	$R_{DS(ON)HI}$	IN to LX	40	180	320	mΩ
Peak current limit threshold	I_{PK}		3.75	5.0		A
Refresh MOSFET “on” resistance	$R_{DS(ON)LO}$	LX to GND		12		Ω
Input under-voltage lockout	V_{UVLO}	V_{IN} rising, hysteresis = 200 mV	3.5		4.2	V
Over-temperature shutdown threshold	T_{SHDN}	Rising edge, hysteresis = 15 °C		160		°C
EN input logic threshold	V_{EN}		0.4		1.7	V
EN input current	I_{EN}	V_{IN} = 24 V	–2.0		40	µA
Soft-start period	t_{SS}			4		ms

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Note 2: The minimum output voltage must be greater than $t_{ON(MIN)} \times f_{OSC} \times V_{IN(MIN)}$ due to duty cycle limitations.

Typical Performance Characteristics

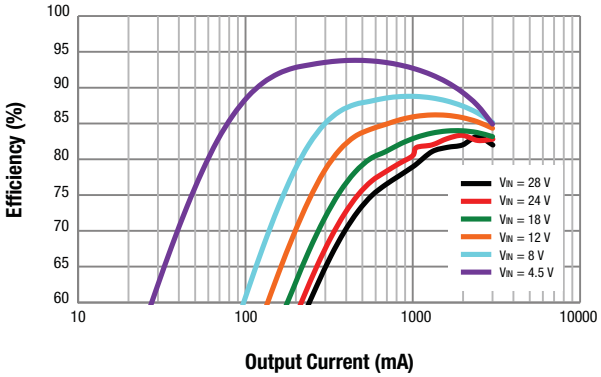


Figure 3. Efficiency vs Output Current (V_{OUT} = 3.3 V)

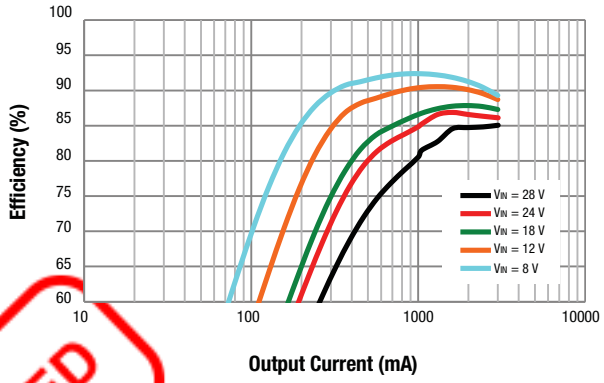


Figure 4. Efficiency vs Output Current (V_{OUT} = 5.0 V)

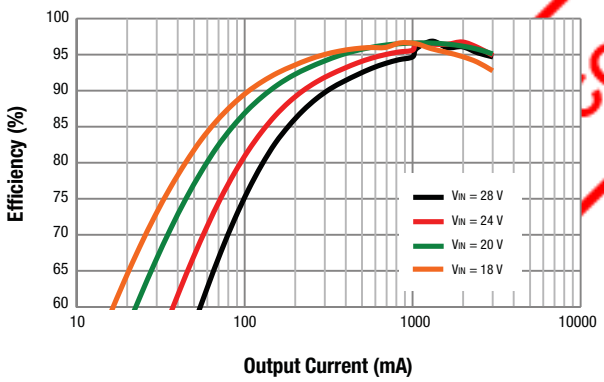


Figure 5. Efficiency vs Output Current (V_{OUT} = 15 V)

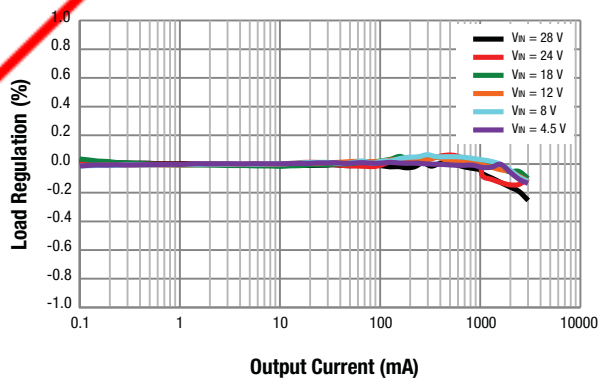


Figure 6. Load Regulation (V_{OUT} = 3.3 V)

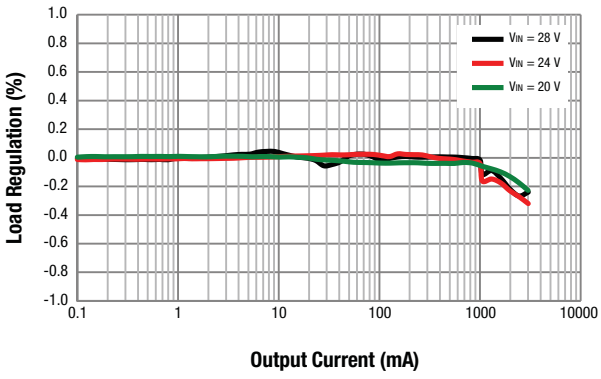


Figure 7. Load Regulation (V_{OUT} = 15 V)

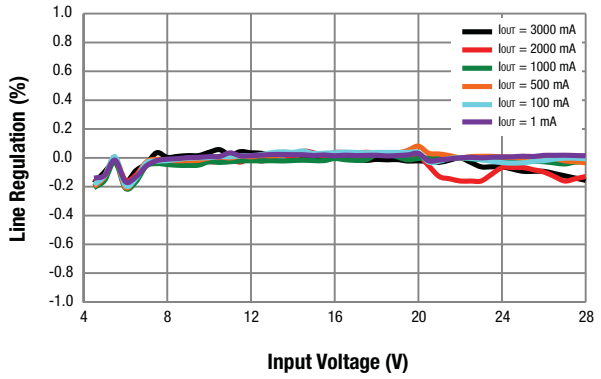


Figure 8. Line Regulation (V_{OUT} = 3.3 V)

Typical Performance Characteristics

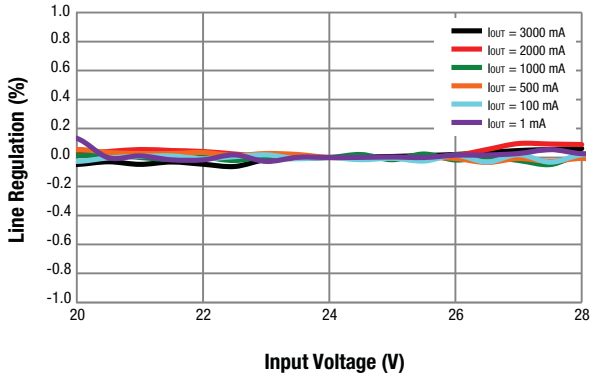


Figure 9. Line Regulation (V_{OUT} = 15 V)

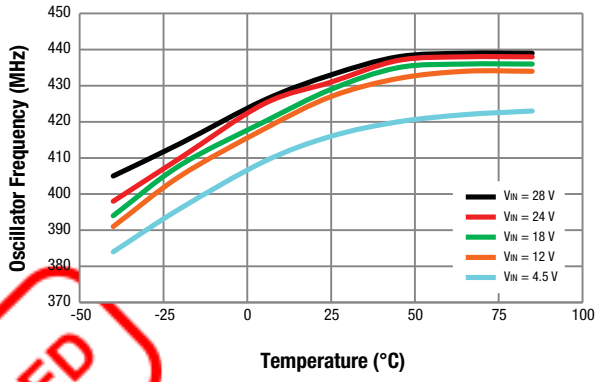


Figure 10. Oscillator Frequency vs Temperature (I_{OUT} = 100 mA)

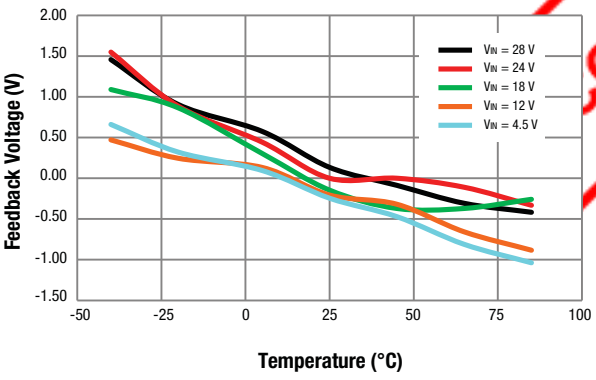


Figure 11. Feedback Voltage Error vs Temperature

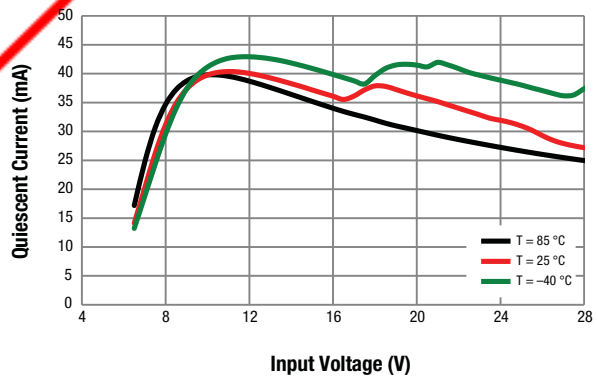


Figure 12. Quiescent Current vs Input Voltage (Switching; No Load)

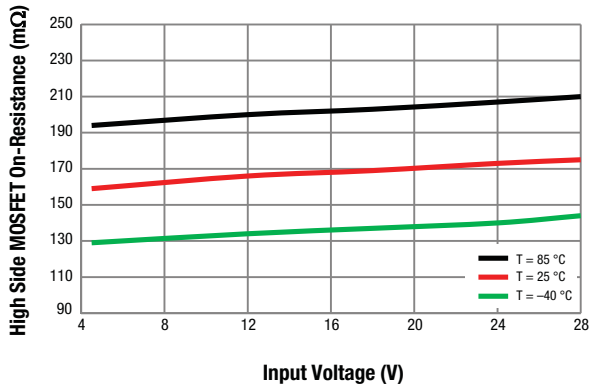


Figure 13. High Side MOSFET On-Resistance vs Input Voltage

Typical Performance Characteristics

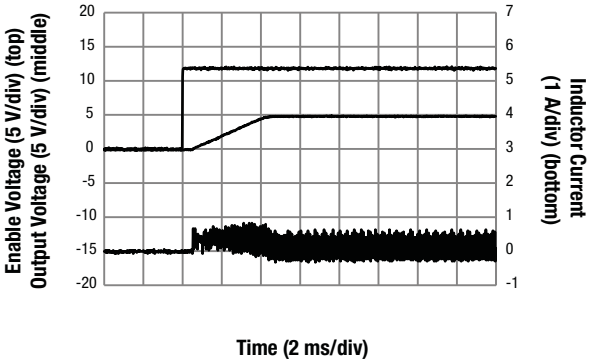


Figure 14. Soft Start (V_{OUT} = 5 V, V_{IN} = 12 V, I_{OUT} = 100 mA)

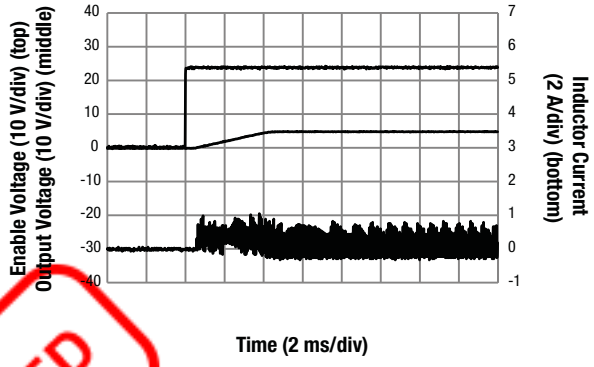


Figure 15. Soft Start (V_{OUT} = 5 V, V_{IN} = 24 V, I_{OUT} = 100 mA)

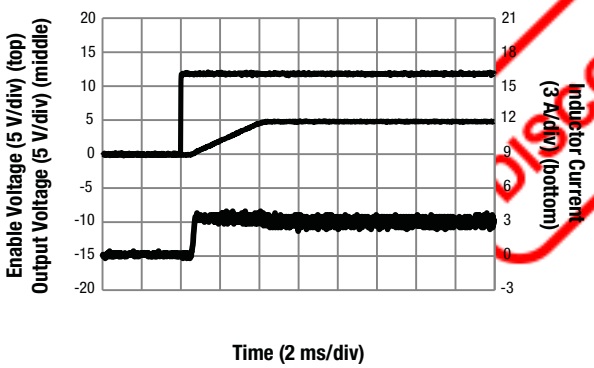


Figure 16. Soft Start (V_{OUT} = 5 V, V_{IN} = 12 V, I_{OUT} = 3 A)

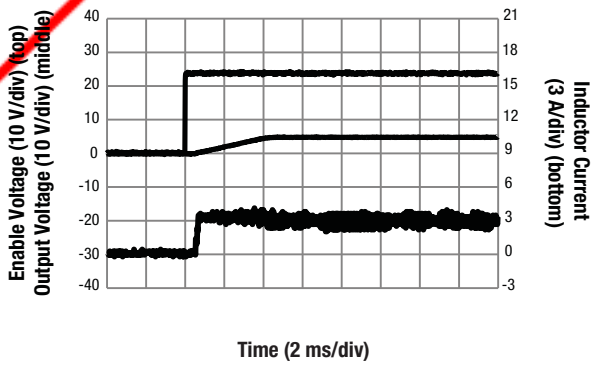


Figure 17. Soft Start (V_{OUT} = 5 V, V_{IN} = 24 V, I_{OUT} = 3 A)

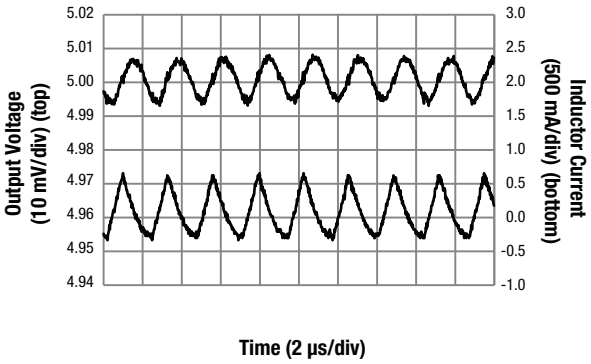


Figure 18. Output Voltage Ripple (V_{OUT} = 5 V, V_{IN} = 12 V, I_{OUT} = 100 mA)

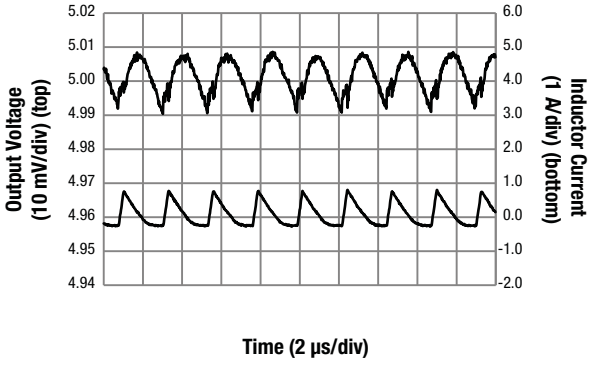


Figure 19. Output Voltage Ripple (V_{OUT} = 5 V, V_{IN} = 24 V, I_{OUT} = 100 mA)

Typical Performance Characteristics

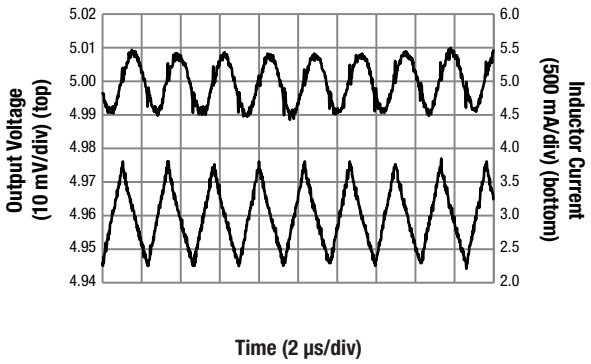


Figure 20. Output Voltage Ripple
(VOUT = 5 V, VIN = 12 V, IOUT = 3 A)

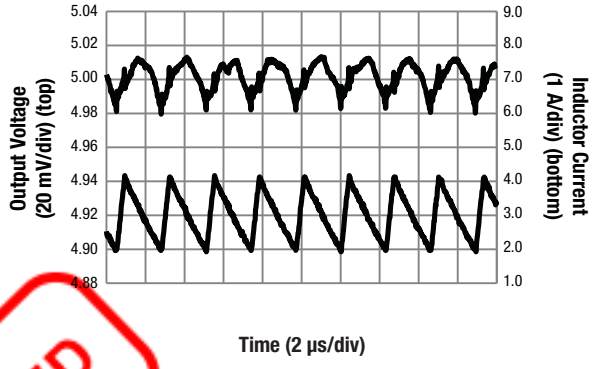


Figure 21. Output Voltage Ripple
(VOUT = 5 V, VIN = 24 V, IOUT = 3 A)

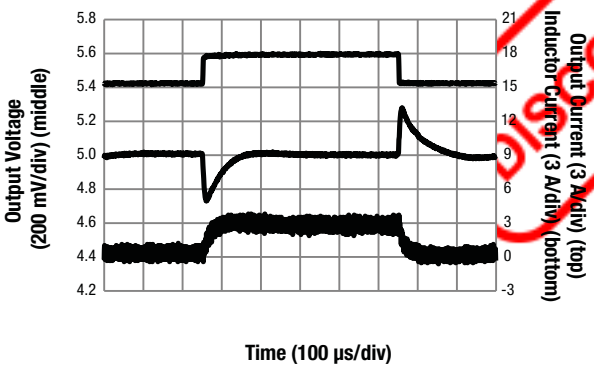


Figure 22. Load Transient
(VOUT = 5 V, VIN = 12 V, IOUT = 0.1 to 3 A)

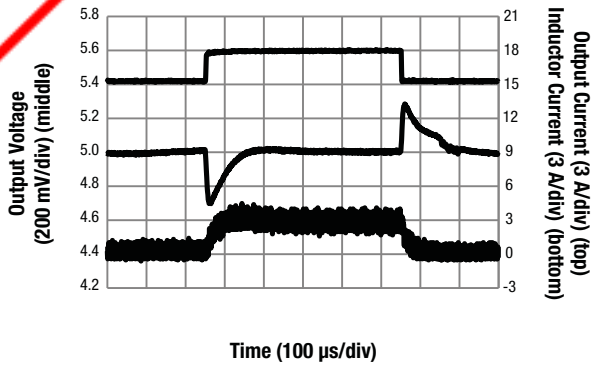


Figure 23. Load Transient
(VOUT = 5 V, VIN = 24 V, IOUT = 0.1 to 3 A)

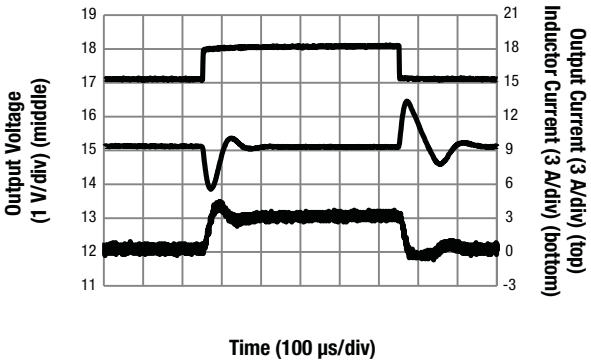


Figure 24. Load Transient
(VOUT = 15 V, VIN = 24 V, IOUT = 0.1 to 3 A)

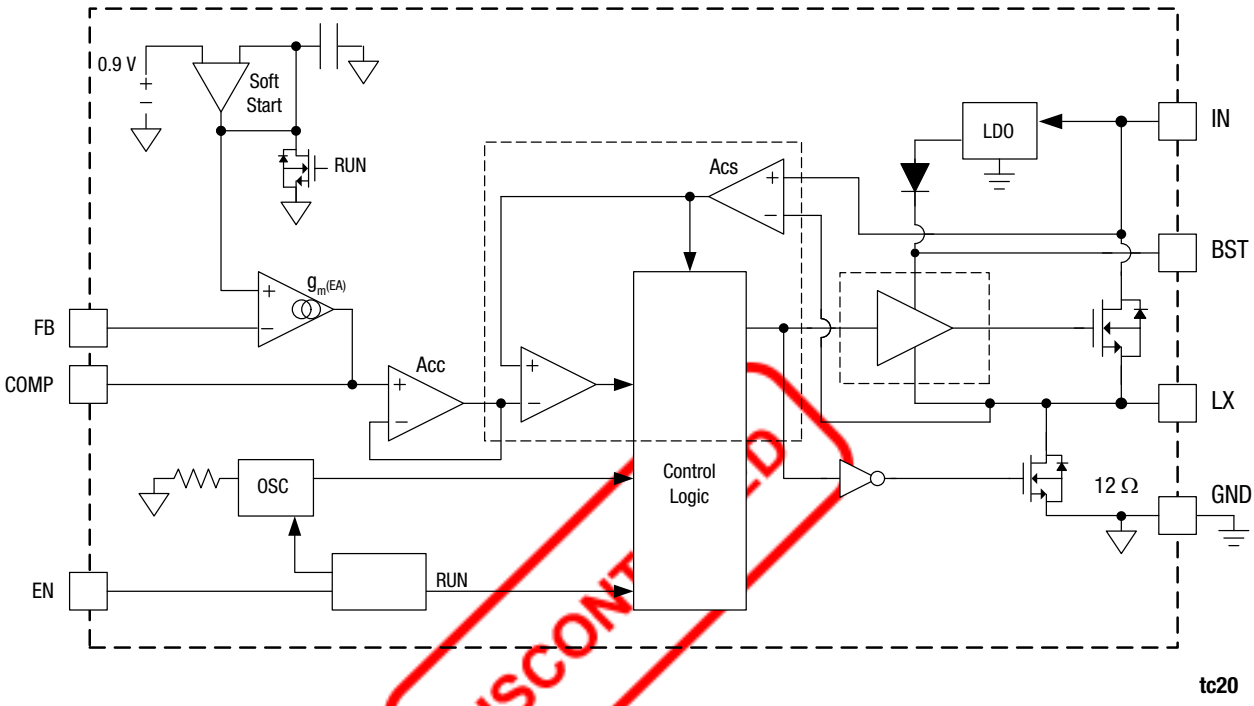


Figure 25. SKY87608 Functional Block Diagram

Functional Description

A functional block diagram is provided in Figure 25.

Control Scheme

The SKY87608 is a non-synchronous, fixed-frequency, current-mode step-down converter. The regulator includes an internal high-side N-channel MOSFET capable of supporting loads up to 3 A. A floating gate driver powers the high-side N-channel MOSFET from an external boot-strap capacitor through the BST pin. The capacitor is charged when LX is pulled low through the rectifier, and the BST capacitor maintains sufficient voltage to enhance the high-side N-channel MOSFET during the on-time. An internal 12 Ω boost capacitor refresh MOSFET allows reliable power-up regardless of the output voltage level.

The SKY87608 supports an adjustable output voltage using an external resistive voltage divider, allowing the output to be set to any voltage between 12% and 80% of the input voltage. The SKY87608 switches at 450 kHz.

Current Limit Protection

The SKY87608 includes protection for overload and short-circuit conditions by limiting the peak inductor current. During the “on” time, the controller monitors the current through the high-side MOSFET. If the current exceeds the peak current-limit threshold (5 A, typical), the controller immediately turns off the high-side MOSFET.

Voltage Soft-Start

The soft-start circuit ramps the reference voltage from ground up to the 0.9 V nominal feedback regulation voltage (see Figure 25). The internal soft-start capacitor sets the soft-start period as 4 ms (typical).

The soft-start is discharged/reset if any of the following occurs: the regulator is disabled (EN pulled low), the input voltage drops below the UVLO threshold, or thermal shutdown is activated.

Thermal Shutdown

The SKY87608 includes thermal protection that disables the regulator when the die temperature reaches 160 °C. The thermal shutdown resets the soft-start circuit and automatically restarts when the temperature drops below 145 °C.

Application Information

To ensure that the maximum possible performance is obtained from the SKY87608, please refer to the following application recommendations for component selection.

Adjustable Output Resistor Selection

The output voltage (V_{OUT}) may be set from 0.9 V to 80% of V_{IN}. The resistive feedback voltage divider sets the output voltage according to the following relationship:

$$R_{FB1} = \left(\frac{V_{OUT}}{0.9V} - 1 \right) \times R_{FB2}$$

RFB1 is rounded to the nearest 1% resistor value. RFB2 is typically selected to be between 10 kΩ and 200 kΩ. The lower resistance improves noise immunity, but results in higher feedback current and reduced efficiency, as shown in Figure 26.

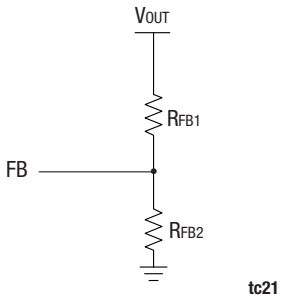


Figure 26. FB Resistor Divider

Table 5 shows the divider resistor value for different output voltages.

Table 5. Resistor Selection for Different Output Voltages

Output Voltage (V)	RFB1 (kΩ) (RFB2 = 20 kΩ)
1.5	13.3
3.3	53.6
5.0	91
8.0	158
10	200
12	249
15	316
18	383
20	422

Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected to make the inductor current down slope to meet the internal slope compensation requirements. The internal slope compensation is designed to be 75% of the inductor current down slope of 5 V output with 6.8 µH inductor.

$$m_c = \frac{0.75 \times V_{OUT}}{L} = \frac{0.75 \times 5V}{6.8\mu H}$$

$$m_c = 0.55 \left(\frac{A}{\mu s} \right)$$

For other output voltages, the inductance can be calculated based on the internal slope compensation requirement and equal to:

$$L = \frac{0.75 \times V_{OUT}}{m_c} = (1.36 \times V_{OUT})\ (\mu H)$$

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions.

The saturation current is a very important parameter for inductor selection. It must be more than the sum of DC current and maximum peak current through the inductor, and the adequate margin is important for safe application. The maximum peak current is given by the following equation:

$$I_{PEAK\_INDUCTOR\_MAX} = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN\_MAX}}\right)}{L \times f}$$

Where L is the inductance and f is the operation frequency.

Some inductors that meet the peak and average current ratings requirements still result in excessive losses due to a high Direct Current Resistance (DCR). Always consider the losses associated with the DCR and their effect on the total regulator efficiency when selecting an inductor. Table 6 shows the recommended inductor examples for different output voltages.

Input Capacitor

Typically, the input impedance is so low (or has other input capacitors distributed throughout the system) that a single 10 µF X7R or X5R ceramic capacitor located near the SKY87608 is sufficient. However, additional input capacitance may be necessary depending on the impedance of the input supply. To estimate the required input capacitance requirement, determine the acceptable input ripple level (VPP) and solve for CIN:

$$C_{IN} = \frac{\left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_{OUT}} - ESR\right) \times f_{SW}} = \frac{D \times (1 - D)}{\left(\frac{V_{PP}}{I_{OUT}} - ESR\right) \times f_{SW}}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when evaluating ceramic bypass capacitors.

In addition to the capacitance requirement, the RMS current rating of the input capacitor must be able to support the pulsed current drawn by the step-down regulator. The input RMS current requirement may be determined by:

$$I_{RMS} = I_{OUT} \times \sqrt{\left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

Table 6. Inductor Selection for Different Output Voltages

VOUT (V)	Inductance (µH)	Part Number	Saturation Current (A)	DCR (mΩ)	Dimension(mm) L×W×H	Manufacturer
1.5	2.5	CDRH8D38NP-2R5N	5.5	17.5	8.3×8.3×4	Sumida
	2.2	744777002	6.5	20	7.3×7.3×4.5	Wurth Elektronik
		DR73-2R2-R	5.52	16.5	7.9×7.9×3.8	Coil Tronics
3.3	4.7	CDRH105RNP-4R7N	6.4	12.3	10.5×10.3×5.1	Sumida
		CDRH10D68NP-4R7N	6.6	9.8	10.5×10.5×7.1	
		7447715004	6.3	16	12×12×4.5	Wurth Elektronik
5	6.8	CDRH105RNP-6R8N	5.4	18	10.5×10.3×5.1	Sumida
		CDRH124NP-6R8M	4.9	23	12.3×12.3×4.5	
		7447715006	4.7	25	12×12×4.5	Wurth Elektronik
10	15	CDRH127NP-15M	4.5	27	12.3×12.3×8	Sumida
		CDRH127/LDHF-150M	5.65	26.4	12.3×12.3×8	
		744771115	4.55	30	12×12×6	Wurth Elektronik
		DR125-150-R	5.69	29.8	13×13×6.3	Coil Tronics
12	18	CDRH127/LDHF-180M	5.1	28	12.3×12.3×8	Sumida
		744771118	4.3	34	12×12×6	Wurth Elektronik
		DR125-180-R	5.32	37.7	13×13×6.3	Coil Tronics
15	22	CDRH127/LDHF-220M	4.7	36.4	12.3×12.3×8	Sumida
		744770122	5.0	43	12×12×8	Wurth Elektronik
		DR125-220-R	4.71	39.6	13×13×6.3	Coil Tronics
18	27	CDRH127/LDHF-270M	4.2	41.6	12.3×12.3×8	Sumida
		744770127	3.8	46	12×12×8	Wurth Elektronik
		7447709270	5.8	40	12×12×10	
20	27	CDRH127/LDHF-270M	4.2	41.6	12.3×12.3×8	Sumida
		744770127	3.8	46	12×12×8	Wurth Elektronik
		7447709270	5.8	40	12×12×10	

The term D × (1 – D) appears in both the input ripple voltage and input capacitor RMS current equations, so the maximum occurs when VOUT = 0.5 × VIN (50% duty cycle). This results in a set of “worst case” capacitance and RMS current design requirements:

$$C_{IN(MIN)} = \frac{1}{4 \times \left(\frac{V_{PP}}{I_{OUT}} - ESR \right) \times f_{SW}}$$

$$I_{RMS(MAX)} = \frac{I_{OUT}}{2}$$

The input capacitor provides a low impedance loop for the pulsed current drawn by the SKY87608. Low Equivalent Series Resistance/Equivalent Series Inductance (ESR/ESL) X7R and X5R ceramic capacitors are ideal for this function. To minimize the stray inductance, the capacitor should be placed as closely as possible to the high-side MOSFET. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple. The proper placement of the input capacitor can be seen in the Evaluation Board layout (see the "Layout Considerations" section of this Data Sheet).

A laboratory test set-up typically consists of two long wires running from the bench power supply to the Evaluation Board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high-Q network that may affect the regulator’s performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the lead inductance of the input power source cannot be reduced to a level that does not affect the regulator performance, a high-ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR/ESL ceramic capacitor. This reduces the input impedance and dampens the high-Q network, stabilizing the input supply.

Output Capacitor

The output capacitor impacts stability, limits the output ripple voltage, and maintains the output voltage during large load transitions. The SKY87608 is designed to work with any type of output capacitor since the controller features externally adjustable compensation (see the "Stability Considerations" and "Compensation Component Selection" sections of this Data Sheet).

The output ripple voltage magnitude is determined by the output capacitor's ability to filter the inductor ripple current. The ripple voltage has two components, capacitive and ESR induced ripple voltage:

$$\Delta V_{OUT(CAP)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

$$\Delta V_{OUT(ESR)} = \Delta I_L \times ESR$$

The capacitive ripple and ESR ripple are phase shifted from each other, but depending on the type of output capacitor chemistry, one of them typically dominates.

After a load step occurs, the output capacitor must support the difference between the load requirement and inductor current. Once the average inductor current increases to the DC load level, the output voltage recovers. Therefore, based on limitations in the ability to discharge the inductor, a minimum output voltage deviation may be determined by the following equation:

$$V_{SOAR(CAP)} = \frac{\Delta I_{OUT}^2 \times L}{2 \times C_{OUT} \times V_{OUT}}$$

$$\Delta V_{SOAR(ESR)} = \Delta I_{OUT} \times ESR$$

Where, V_{SOAR} is the output voltage overshoot and undershoot deviation. Bandwidth and gain limitations (depending on output capacitor and compensation component selection) may result in larger output voltage deviations.

The ceramic output capacitor provides low ESR and low ESL, resulting in low output ripple dominated by the capacitive ripple voltage ($\Delta V_{OUT(CAP)}$). However, due to the lower capacitance value, the load transient response is significantly worse. Therefore, ceramic output capacitors are generally recommended only for designs with soft load transients (slow di/dt and/or small load steps).

Tantalum and electrolytic capacitors provide a high-capacitance, low-cost solution. The bulk capacitance provides minimal output voltage drop/soar after load transients occur.

Stability Considerations

The SKY87608 uses a current-mode architecture, which relies on the output capacitor and a series resistor-capacitor network on the COMP pin for stability. COMP is the output of the transconductance error amplifier, so the RC network creates a pole-zero pair used to control the gain and bandwidth of the control loop.

The DC loop gain (A_{DC}) is set by the voltage gain of the internal transconductance amplifier ($A_{EA} = g_{M(EA)} \times R_{OUT} = 3000$ V/V), the compensation gain ($A_{CC} = 1$ V/V), and the current-sense gain ($A_{CS} = 1$ V/V):

$$A_{DC} = \frac{V_{FB}}{V_{OUT}} \times \frac{A_{CC}}{A_{CS} \times R_{DS(ON)}} \times A_{EA} \times R_{LOAD}$$

Where V_{FB} is the 0.9 V feedback voltage, V_{OUT} is the output voltage determined by the feedback resistors, $R_{DS(ON)}$ is the "on" resistance of the high-side N-channel MOSFET, and R_{LOAD} is the output load resistance ($R_{LOAD} = V_{OUT} / I_{OUT}$).

Since the output impedance is a function of the load current and output voltage, the equation may be rewritten independent of the V_{OUT} term:

$$A_{DC} = \frac{V_{FB}}{I_{OUT}} \times \frac{A_{CC}}{A_{CS} \times R_{DS(ON)}} \times A_{EA}$$

Additionally, the high-side "on" resistance $R_{DS(ON)}$ is inversely proportional to the maximum output current (I_{OUT}) due to the peak current limit. This effectively limits the typical value of A_{DC} to a value of 360 V/V (51 dB).

The control loop has two dominant poles: one created by the output capacitor (C_{OUT}) and load resistance, and the other formed by the total compensation capacitance ($C_{CC1} + C_{CC2}$) and the error amplifier transconductance ($g_{M(EA)} = 570$ µA/V):

$$f_{P1} = \frac{1}{2\pi \times R_{LOAD} \times C_{OUT}} = \frac{I_{OUT}}{2\pi \times V_{OUT} \times C_{OUT}}$$

$$f_{P2} = \frac{g_{m(EA)}}{2\pi \times A_{EA} \times (C_{CC1} + C_{CC2})}$$

However, the system also has two zeros in the control loop: one created by the series compensation resistor (R_{COMP}) and capacitor (C_{CC1}), and the other formed by the output capacitor and its parasitic series resistance (ESR):

$$f_{Z1} = \frac{1}{2\pi \times R_{COMP} \times C_{CC1}}$$

$$f_{Z2} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

The ESR zero is highly dependent on the type of output capacitors being used (ceramic vs tantalum), and may not occur before crossover. If the ESR zero occurs low enough, the compensation zero formed by RCOMP may be placed at crossover to avoid stability problems.

However, if both zeros are required below crossover, a third pole is needed to maintain stability. This third pole can be added by including another compensation capacitor (CCC2 in Figure 1) in parallel with the main series RC network:

$$f_{P3} = \frac{1}{2\pi \times R_{COMP} \times \left(\frac{C_{CC1} \times C_{CC2}}{C_{CC1} + C_{CC2}}\right)}$$

If $C_{CC2} << C_{CC1}$, the third pole is simplified to:

$$f_{P3} = \frac{1}{2\pi \times R_{COMP} \times C_{CC2}}$$

To safely avoid the Nyquist pole (half the switching frequency), the crossover frequency should occur between 1/20th and 1/5th of the switching frequency. Lower crossover frequencies result in slower transient response speed, while higher crossover frequencies could result in instability, as shown in Figure 27.

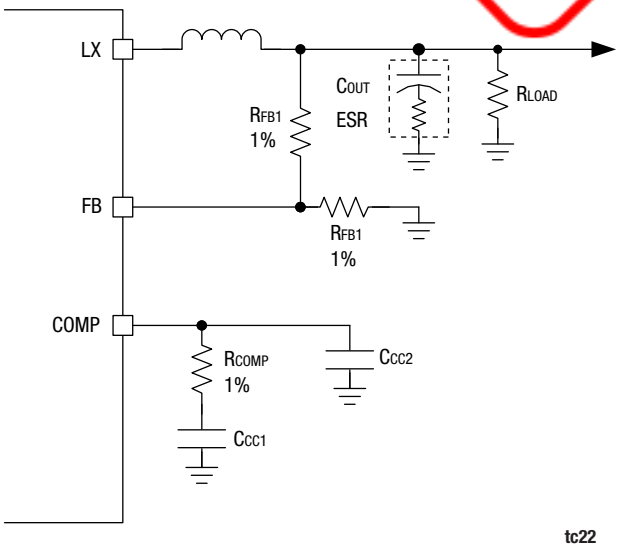


Figure 27. Compensation Components

Compensation Component Selection

This is peak current mode control. An R-C series network (or type II) compensation is applied at the transconductance amplifier output (COMP).

- ROUT(EA) is the output impedance of the transconductance error amplifier.
- N is the scaling factor of output current, ISEN = IOUT/N (N = 1 in this case).
- RSEN is the high side current sensing resistor, RSEN = RDS(HS) in this case.

There is already a 90° phase shift at very low frequencies, ωP1. Compensating the 2nd pole ωP2 with 1st zero ωZ1, the unity gain frequency can be simplified as:

$$f_T = \frac{V_{REF} \times (g_m \times R_{COMP})}{2\pi \times V_{OUT} \times C_{OUT} \times R_{SEN}}$$

Set the unity gain frequency far away from the switching frequency to avoid any switching noise in the voltage loop, $f_T = f_{SW}/20$.

$$R_{COMP} = 2\pi f_T \times \frac{V_{OUT} \times C_{OUT} \times R_{SEN}}{V_{REF} \cdot g_m}$$

$$C_{CC1} = \frac{C_{OUT} \times R_{L(MIN)}}{R_{COMP}}$$

The ESR zero ωZ2 is used to cancel the high frequency pole ωP3.

$$C_{CC2} = \frac{C_{OUT} \times R_{ESR}}{R_{COMP}}$$

g_m = 570 µA/V, $g_m \times R_{OUT(EA)}$ = 3000 V/V, RSEN = 100 mΩ, COUT = 22 µF, and RESR = 10 mΩ.

For VOUT = 3.3 V, RCOMP = 2 kΩ, CCC1= 10 nF, and CCC2 = 100 pF.

For VOUT = 5 V, RCOMP = 3 kΩ, CCC1= 10 nF, and CCC2 = 56 pF.

For VOUT = 15 V, RCOMP = 9.1 kΩ, CCC1= 10 nF, and CCC2 = 22 pF.

Table 7 gives the recommended compensation value for different output voltages.

Table 7. Recommended Compensation Values

VOUT (V)	RCOMP (kΩ)	CCC1 (nf)	CCC2 (pf)
1.5	1.0	10	270
3.3	2	10	100
5	3	10	56
10	6.2	10	33
12	7.5	10	33
15	9.1	10	22
18	10	10	22
20	12	10	22

The type of output capacitor determines how the compensation components should be selected. With large tantalum and electrolytic capacitors, the output capacitor pole dominates the control loop design. Alternatively, small low-ESR ceramic capacitors rely on the compensation capacitor to generate the dominant pole.

Bootstrap Capacitor Selection

To fully turn on the high side N-channel MOSFET, a bootstrap capacitor is connected between the BST pin and the LX pin. During the off time, the switching node is pulled to ground and the bootstrap capacitor charges up to approximately 5 V through an internal diode (see Figure 25). The bootstrap capacitor should be a 22 nF to 100 nF ceramic capacitor with a 10 V or greater voltage rating.

Diode Selection

To achieve maximum efficiency, a low-V_F Schottky diode is recommended.

$$I_{RMS\_DIODE} = \sqrt{\frac{V_{IN} - V_{OUT}}{V_{IN}} \times \left(I^2_{OUT} + \frac{\Delta I^2_L}{12} \right)}$$

Where ΔI_L is the peak-to-peak value of inductor current. Select a diode with a DC rated current equal to the current RMS of the diode with an adequate margin for safe use.

Table 8 lists a few recommended Schottky diodes.

Thermal Calculations

There are three types of losses associated with the SKY87608 step-down converter: switching losses, conduction losses, and quiescent current losses. The conduction losses are associated with the $R_{DS(ON)}$ characteristics of the internal high-side MOSFET. The switching losses are dominated by the gate charge and parasitic capacitance of the high-side MOSFET. Under full load conditions, the total power loss within the SKY87608 may be estimated by:

$$P_{TOTAL} = \left(\frac{I_{OUT}{}^2 \times R_{DS(ON)H} \times V_{OUT}}{V_{IN}} \right) + (t_{SW} \times f_{SW} \times I_{OUT} + I_Q) \times V_{IN}$$

where I_Q is the step-down converter quiescent current, and t_{SW} is the turn-on/off time of the MOSFET used to estimate the full load step-down converter switching losses. Since on time, quiescent current, and switching losses all vary with input voltage, the total power losses within the SKY87608 should be investigated over the complete input voltage range.

The maximum junction temperature can be derived from the θ_{JA} for the SOP-8L-EP package, which is 41 °C/W.

$$T_{J(MAX)} = P_{TOTAL} \times \theta_{JA} + T_A$$

Layout Considerations

The following guidelines should be used to help ensure a proper layout.

1. Connect the input capacitor as close as possible to the drain of the high-side N-channel MOSFET and the anode of the Schottky diode (and/or source of the low-side N-channel MOSFET). Keep this loop compact to reduce the switching noise.
2. Connect C_{OUT} and L1 as close as possible. The connection of L1 to the LX pin should be as short as possible and made at the source of the high-side N-channel MOSFET for current-sense accuracy.
3. Separate the feedback trace or FB pin from any power trace and connect as close as possible to the load point. Sensing along a high-current load trace degrades DC load regulation.
4. Minimize the resistance of the trace from the load return to PGND. This helps to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. Connect PGND to the exposed pad to enhance thermal impedance.

Evaluation Board Description

The SKY87608 Evaluation Board schematic diagram is provided in Figure 28. The PCB layer detail is shown in Figures 29 and 30. Component values for the SKY87608 Evaluation Board are listed in Table 9.

Package Information

Package dimensions and tape & reel dimensions are shown in Figures 31 and 32.

Table 8. SKY87608 Schottky Diode Selection

Part Number	V_R (V)	V_F (V)	I_F (A)	Package	Manufacturer
B340A	40	0.5 @ 3 A	3	SMA	VISHAY
SS34	40	0.46 @ 3 A	3	SMC	Fairchild
MBRS540	40	0.5 @ 5 A	5	SMC	ON
CMSH5-40	40	0.55 @ 5 A	5	SMC	Central

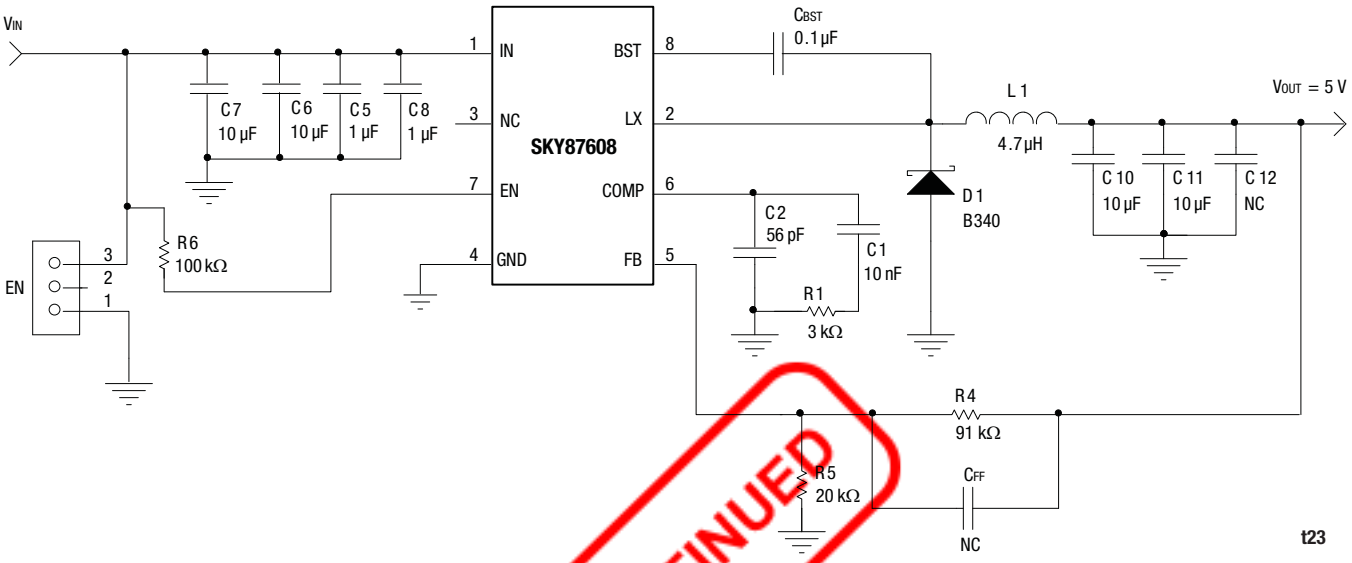


Figure 28: SKY87608 Standard Application Circuit Schematic

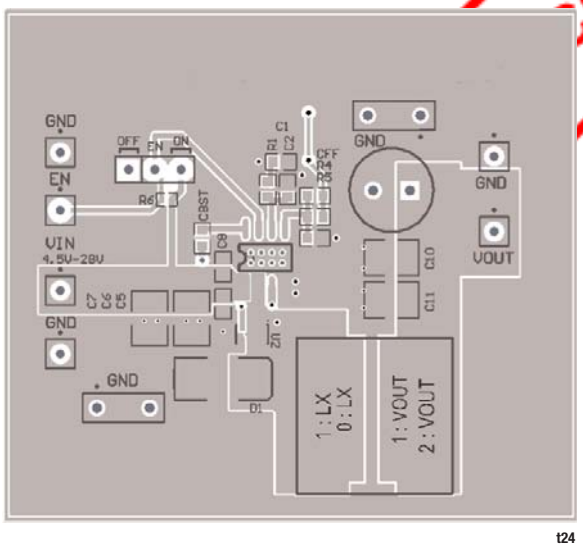


Figure 29: SKY87608 Evaluation Board Top Side Layout

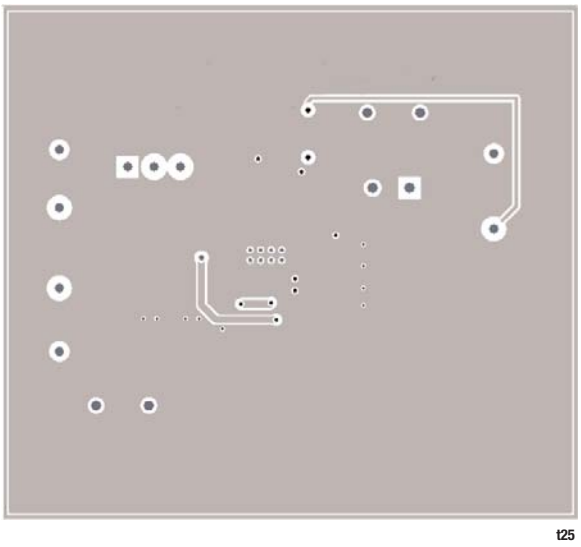
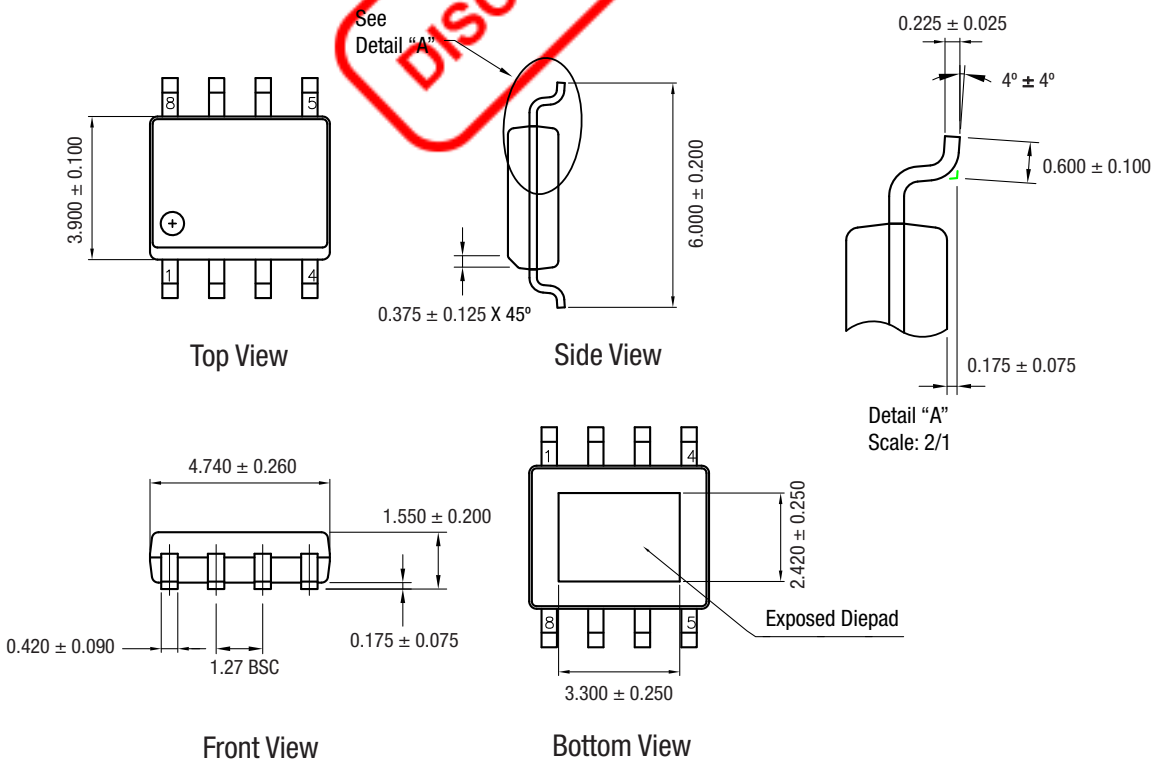


Figure 30: SKY87608 Evaluation Board Bottom Side Layout

Table 9. SKY87608 Standard Application Circuit Bill of Materials (BOM)

Component	Part Number	Description	Manufacturer
U1	SKY87608-11-577LF	Step-down converter	Murata
C1	GRM188R71C103K	Capacitor, ceramic, 10 nF, 0603 X7R, 16 V, 10%	Murata
C2	GRM1885C1H560J	Capacitor, ceramic, 56 pF, 0603 C0G, 50 V, 5%	Murata
C5,C8	GRM188R61H105KAALD	Capacitor, ceramic, 1 µF, 0603 X5R, 50 V, 10%	Murata
C6, C7, C10, C11	GRM32ER7YA106K	Capacitor, ceramic, 10 µF, 1210 X7R, 35 V, 10%	Murata
CBST	GRM188R71C104K	Capacitor, ceramic, 0.1 µF, 0603 X7R, 16 V, 10%	Murata
C12		Not populated	
CFF			
R1	RC0603FR-073KL	Resistor,3 kΩ, 1/10 W, 1%, 0603 SMD	Yageo
R4	RC0603FR-0791KL	Resistor, 91 kΩ, 1/10 W, 1%, 0603 SMD	Yageo
R5	RC0603FR-0720KL	Resistor, 20 kΩ, 1/10 W, 1%, 0603 SMD	Yageo
R6	RC0603FR-07100KL	Resistor, 100 kΩ, 1/10 W, 1%, 0603 SMD	Yageo
D1	B340A	Diode, 40 V, 3 A, SMA	Vishay
L1	7447715006	Inductor, 6.8 µH, 4.7 A	Wurth Elektronik



All dimentions are in millimeters.

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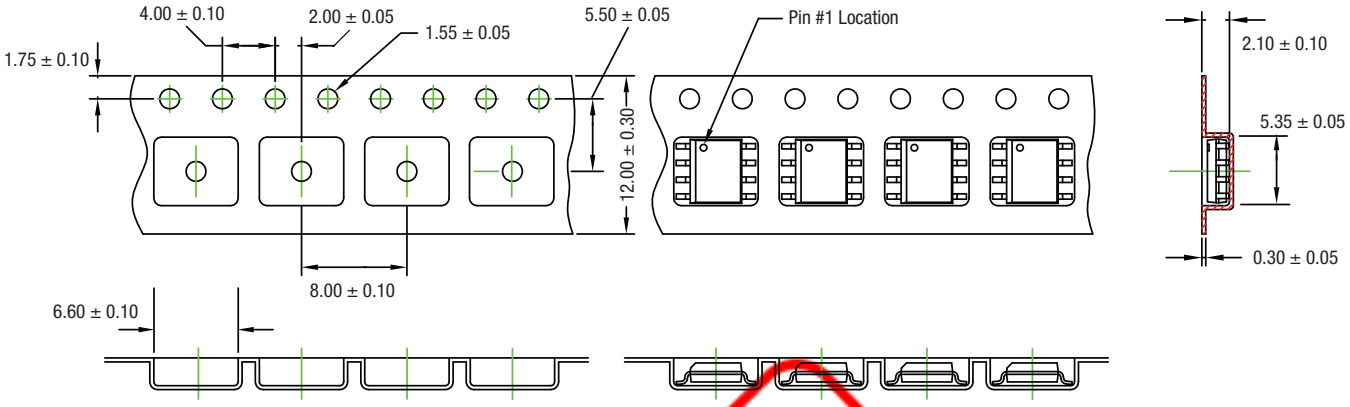
Figure 31. SKY87608 8-pin SOP-8L-EP Package Dimensions



All dimensions are in millimeters.

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Figure 32. SKY87608 Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number (Note 1)	Evaluation Board Part Number
SKY87608 Step Down DC-DC Converter	**SKY87608-11-577LF**	SKY87608-11-577LF-EVB

Note 1: Sample stock is generally held on the part number listed in **BOLD**.